Amendments to the Specification:

Please replace the paragraph beginning on page 1, line 13, and ending on page 2, line 2, of the specification with the following amended paragraph:

Figure 1 is a block diagram illustrating a first related ~~out~~ art connection construction between exchangers. Exchangers 10, 13 are separately connected to MUX/DEMUXs 11, 12 through 63 E1 links. The MUX/DEMUXs 11,12 are connected to each other through an STM-1 link. The 63 E1 signals outputted from the exchanger 10 are thus multiplexed into an STM-1 signal in the MUX/DEMUX 11 and then transmitted to the STM-1 link. The MUX/DEMUX 12 demultiplexes the transmitted STM-1 signal into the original 63 E1 signals and outputs them to the exchanger 13. Accordingly, E1 base communication between exchangers 10,13 can be performed.

Please replace the paragraph beginning on page 2, line 17, and ending on page 3, line 4, of the specification with the following amended paragraph:

In operation, the framers 100-1~100-4 perform interface operations with respect to the 4 E1 links respectively, and read the signaling data stream from the corresponding link. The data stream is then stored in its register. Once the signaling data streams are stored, the CPU 102 outputs control signals to the framers 100-1~100-4 and reads the signaling data streams from the register of the each framers 100-1~100-4. Accordingly, as depicted in

Figure 3A, for one link, the signaling data streams about 32 channels (time slot) are read from the register, and are stored in the LM 101. The above operations for the other E1 links are repeated.

Please replace the paragraph beginning on page 3, line 5, and ending at line 10, of the specification with the following amended paragraph:

When the signaling data streams storing is completed, the CPU 102 reads the signaling data streams stored in the LM 101, reformats it into the report data depicted in Figure 3B, and stores it on the CM 103. The above operation is performed in 8msec real time cycle, and the processing for the signaling data stream of the 4 links has to be completed in 8msec. Accordingly, the upper processor 104 performs the control operation for the STM-1 interface block by accessing the report data stored in the CM 103.

Please replace the paragraph beginning on page 6, line 13, and ending on page 7, line 2, of the specification with the following amended paragraph:

To further achieve at least these objects in whole or in parts, there is provided a channel associated signaling (CAS) data processing apparatus of a STM-1 interface block, comprising a plurality of framers, coupled to extract signaling data streams from a plurality of E1 links; a CPU, configured to output a start signal to control signaling data processing; a signaling

processing unit, which is activated by the start signal to reformat the signaling data streams inputted from the plurality of framers and output report data in an order of each link; a CPU; interface which interfaces the CPU and the signaling processing unit; and a common memory (CM) interface, which interfaces the CAS signaling processing unit with a common memory to provide the report data to the common memory.

Please replace the paragraph beginning on page 9, line 8, and ending at line 11, of the specification with the following amended paragraph:

Figure 5 depicts the preferred embodiment of the CAS data processing apparatus of the STM-1 interface block of the present invention~~, it comprises~~. As shown, the apparatus includes a plurality of framers 200-1~200-21, a LM (Local Memory) 201, a CPU 202, a CM (Common Memory) 203 and a CAS signaling processing unit 204.

Please replace the paragraph beginning on page 11, line 1, and ending at line 6, of the specification with the following amended paragraph:

The signaling processing unit 31 generates a low level CMPE (Common Memory Process Enable signal) every 4 time periods, as shown in Figure 6E. Next, as shown in Figures 6H, 6J, and 6K, a ~~SDRE~~ SDLE (Signaling Data Latch Enable signal), a CMCS (Common Memory Chip Select signal), and a CMWE (Common Memory Write Enable

signal) are generated by being synchronized with the CMPE signal. Herein, the CMCS and CMWE are operated in a write mode by the CM 203.

Please replace the paragraph beginning on page 11, line 7, and ending at line 14, of the specification with the following amended paragraph:

Accordingly, when the ~~SDRE~~ SDLE is at a low level depicted (Figure 6H), the signaling processing unit 31 reads each channel's (time slot) data from the signaling data stream in accordance with the read pulse signal (MCLK), depicted in Figure 6F. The signaling processing unit 31 temporarily stores the read data on ~~a~~ an inner circuit. For example, as depicted in Figure 6G, the signaling processing unit 31 reads and stores the time slot #0 data "0000". The read pulse signal (MCLK) is preferably the system clock signal divided into two, and a cycle of it is same as an interval of one time slot. Thus the read pulse cycles through two times for every time slot.

Please replace the paragraph beginning on page 13, line 6, and ending at line 9, of the specification with the following amended paragraph:

Moreover, the CAS data processing apparatus of the STM-1 interface block as described herein can reduce the load of the CPU drastically by processing the CAS signaling

data though the logic of the separate ~~hard~~hardware. Accordingly it is possible to construct the system with the low speed CPU, thus the manufacture cost can be reduced.